

FIG. 1a

<u>130</u>

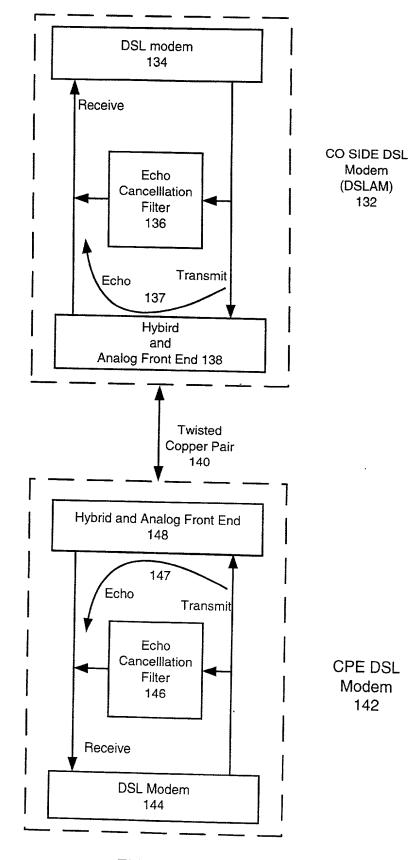


FIG. 1b

<u>150</u>

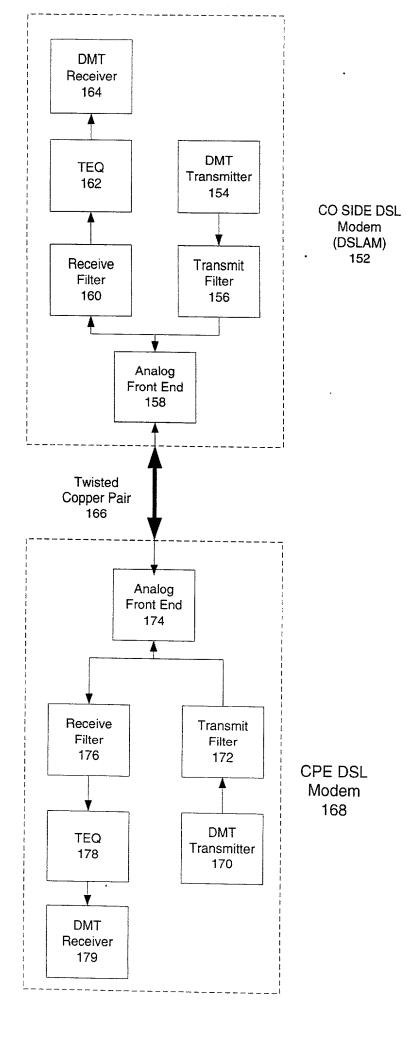


FIG. 1c

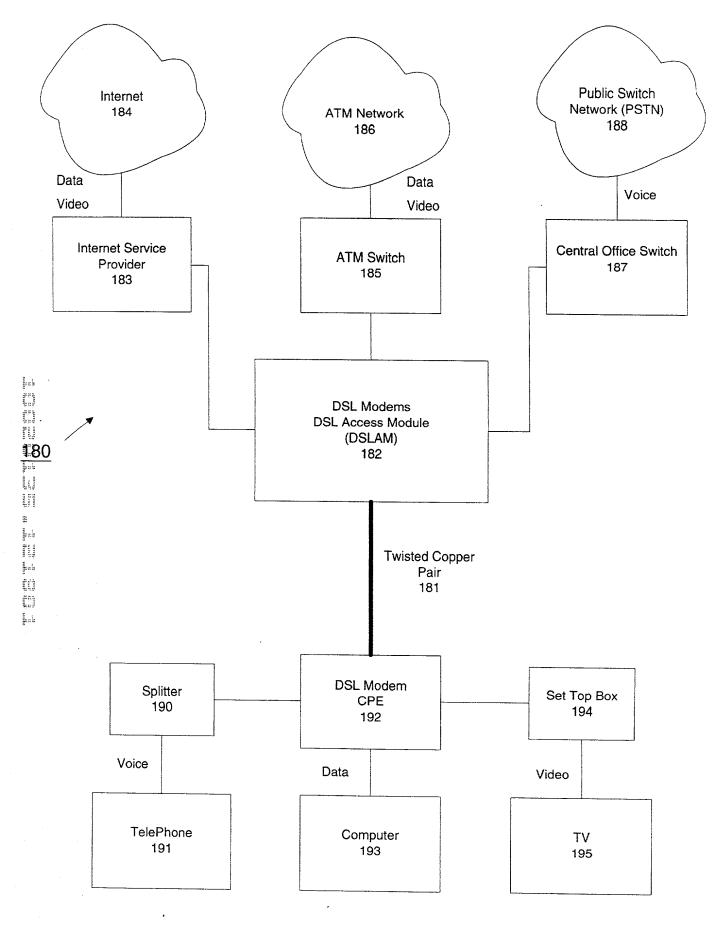


FIG. 1d

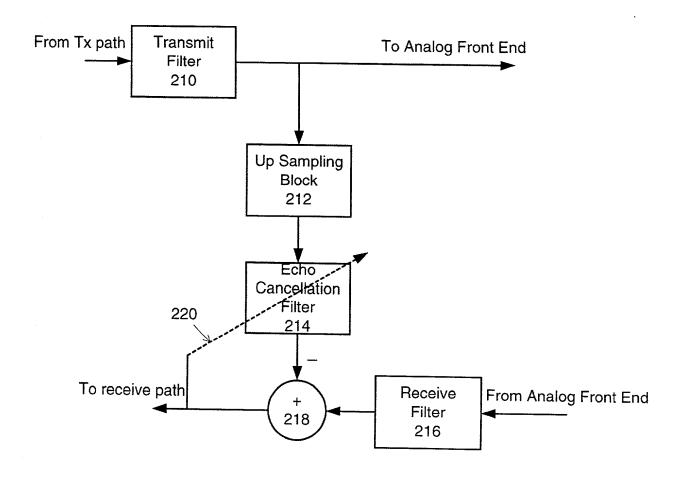


FIG. 2

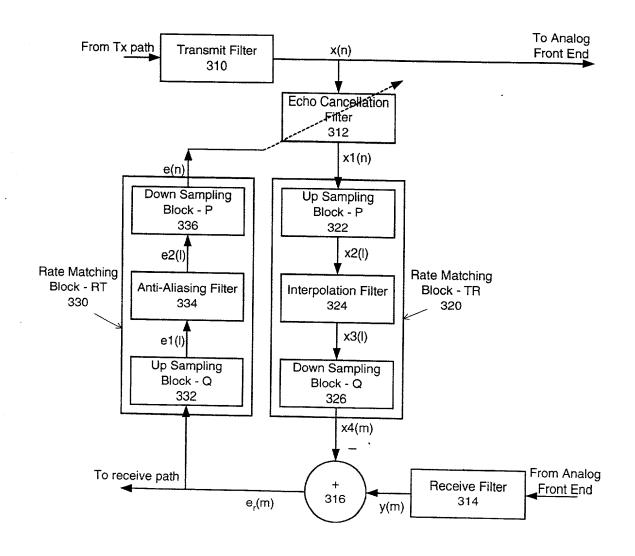
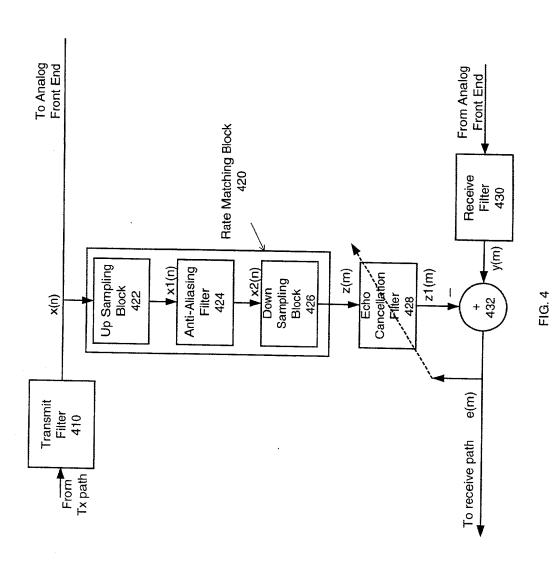


FIG. 3



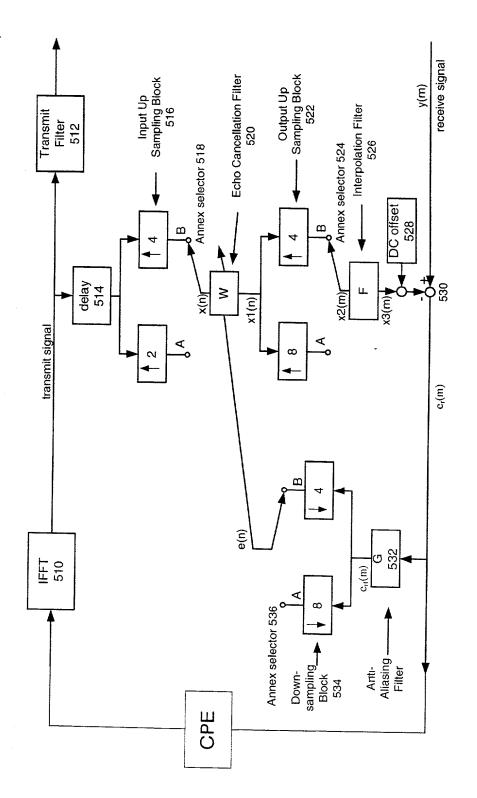
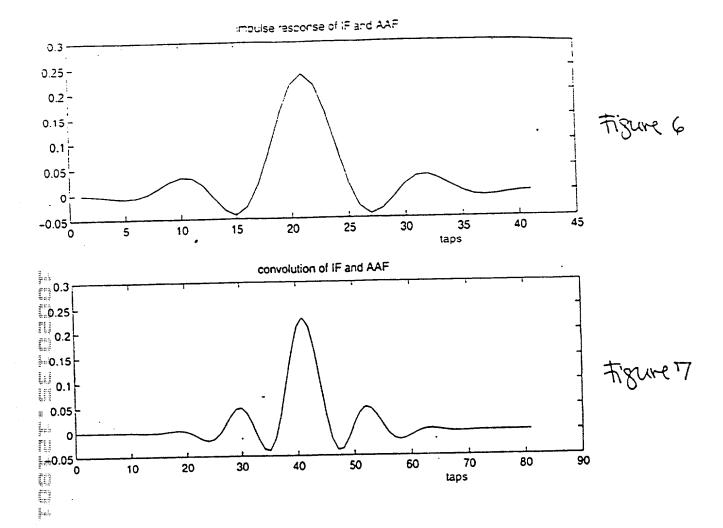
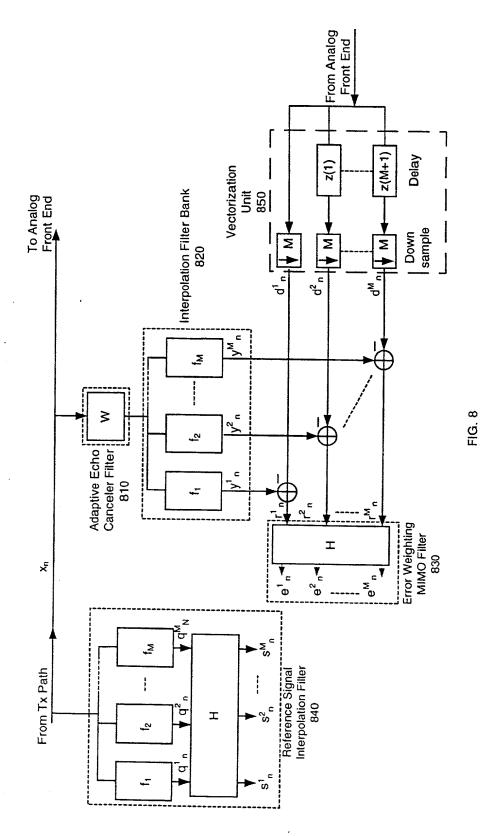


FIG. 5





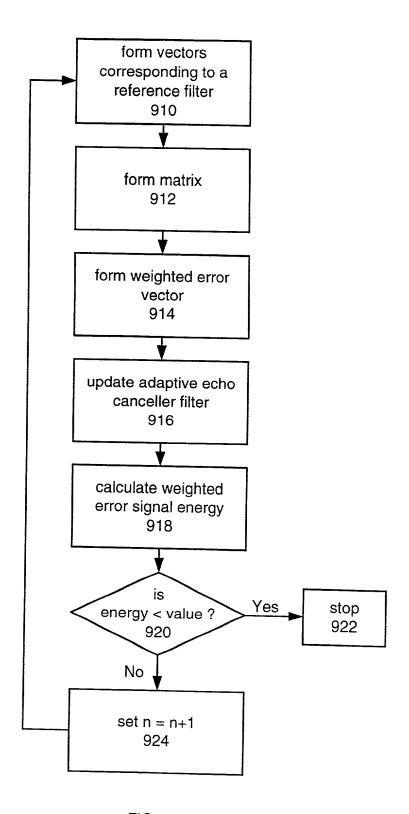


FIG. 9

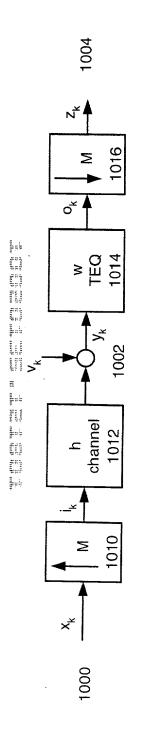


FIG. 10a

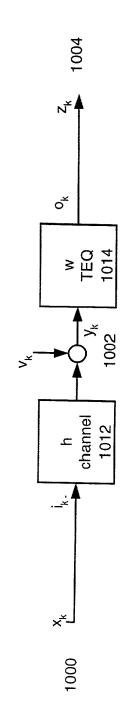


FIG. 10b

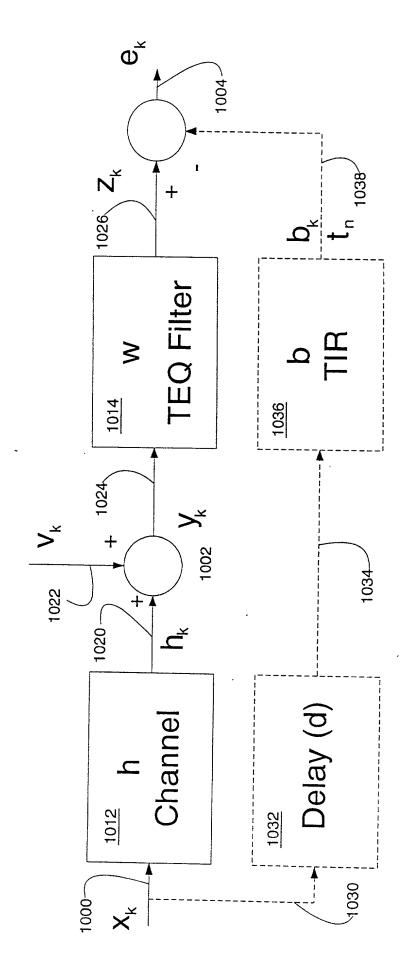


Fig. 10c

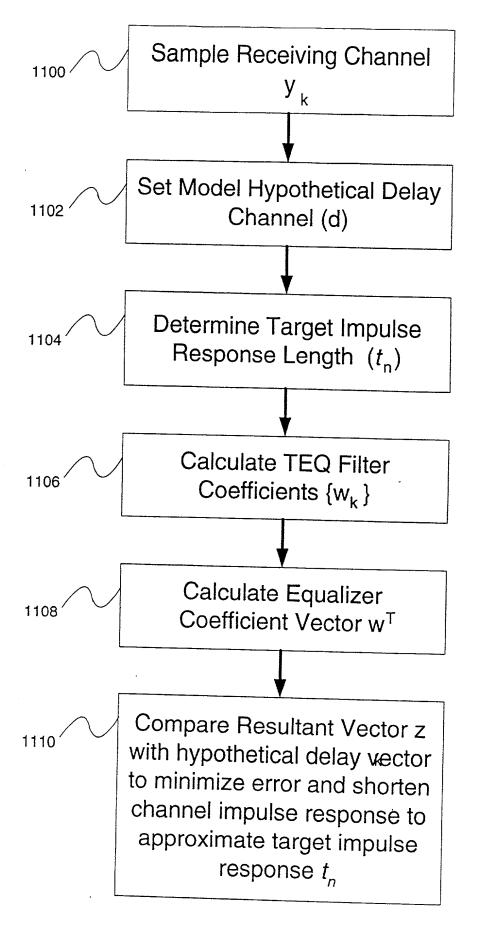


Fig. 11

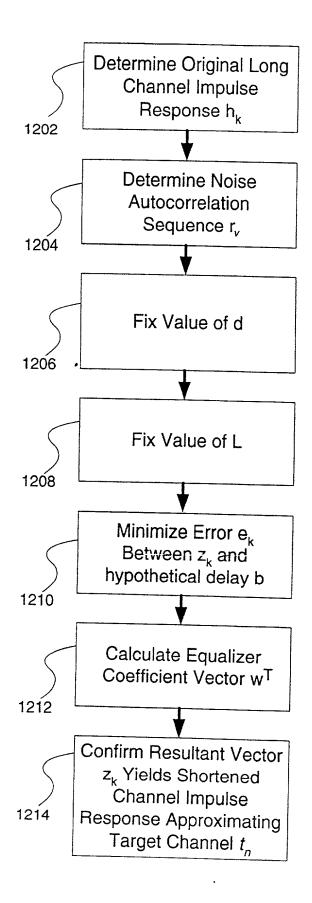


Fig. 12

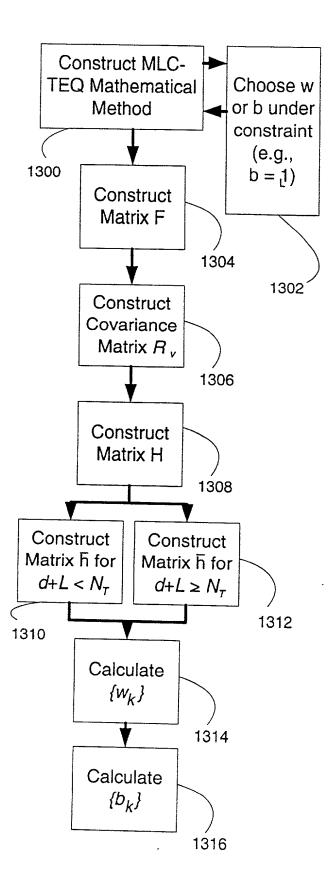


Fig. 13

1400

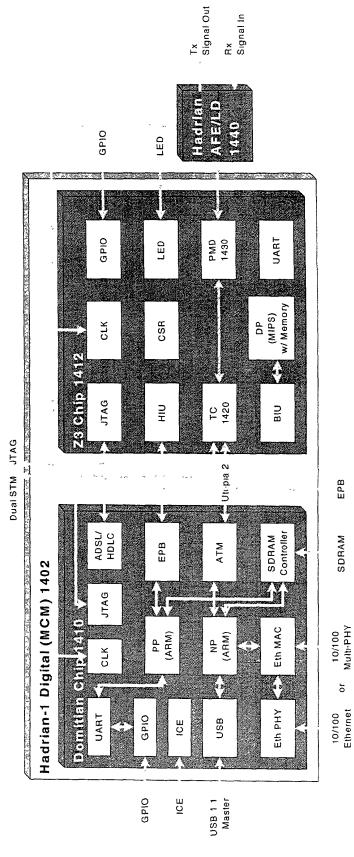


FIG. 14a

EPB

SDRAM

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Dual STM JTAG

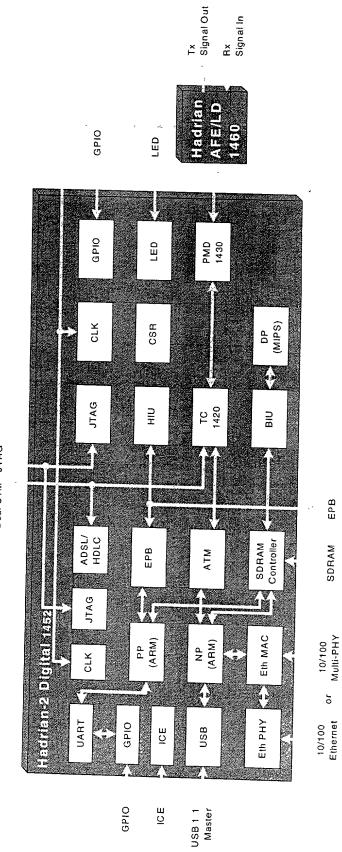


FIG. 14b

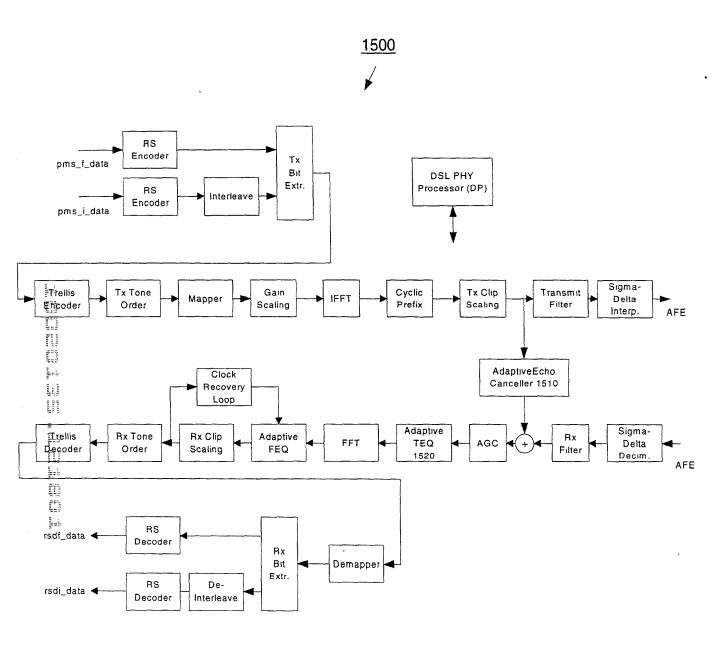


FIG. 15



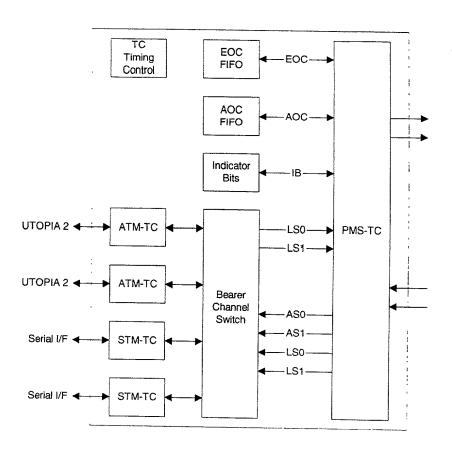


FIG. 16

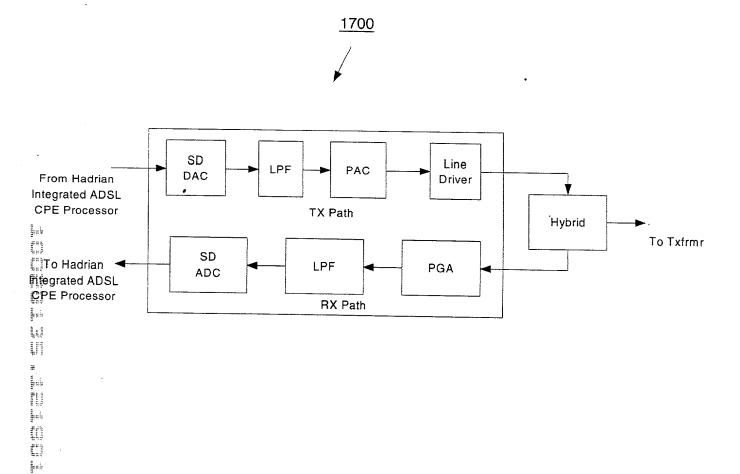


FIG. 17

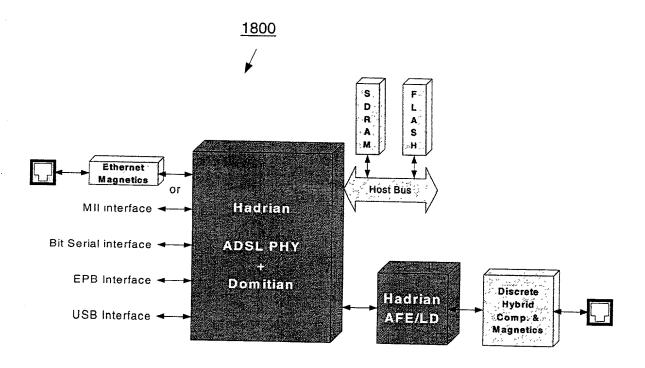


FIG. 18a

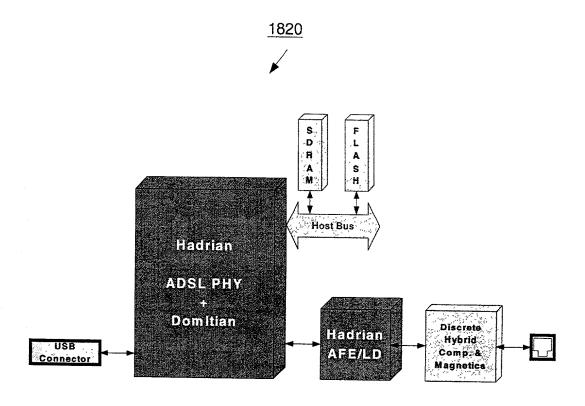


FIG. 18b

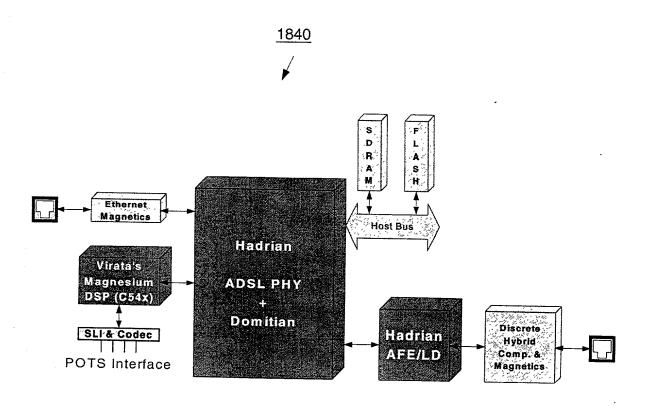


FIG. 18c